Harmonic Power Standard of VTT MIKES

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***Abstract*— This paper describes the new single-phase harmonic power standard developed at VTT MIKES. The standard is based on a custom digitizer, which is designed for both laboratory and on-site power metrology. Test signals are generated using a dual-channel arbitrary function generator, a voltage amplifier, and a transconductance amplifier. The reference voltage and current measurements are, respectively, based on a capacitive–resistive voltage divider and two different types of resistive shunt designs. Thorough characterization of the components is presented. Finally, a tentative uncertainty budget is drawn up for frequencies 53 Hz, 1 kHz, 10 kHz on power factors 1.0 and 0.0. The standard has an expanded uncertainty of 32 and 157 μW/VA at 10 kHz for power factors of 1.0 and 0.0, respectively.**

***Index Terms*— Current measurement, measurement, measurement standards, measurement uncertainty, power measurement, voltage measurement.**

I. Introduction

INCREASED harmonic pollution in the electricity grid is driving the need for utilization of power quality analyzers to quantify the disturbances. To support this, many national metrology institutes have been gearing up to provide traceable power standards up to and beyond hundreds of kilohertz [1]–[3]. This paper describes the setup developed at VTT MIKES for single-phase power calibration up to 10 kHz.

II. Measurement Setup

The measurement setup previously published in [4] is shown in Fig. 1. A two-channel arbitrary function generator (ARB) is used for generating repetitive test signals either single tone or with programed harmonic content. The test voltage up to 350 V is generated with a commercially available broadband voltage amplifier (VA). Respectively, the current signal up to 20 A is generated using a commercially available transconductance amplifier. Test signal path gains and phase responses are compensated in the ARB settings based on the reference measurement used in the setup. Reference voltage measurement is done with a 50:1 voltage divider and current measurement with a set of resistive shunts ranging from 75 mΩ to 2 Ω. The voltage and current inputs of the device under calibration are, respectively, connected in parallel to the reference voltage divider and in series with the reference current shunt. This paper extends the work presented in [4] by showing details and measurement results of the reference equipment in the setup in Fig. 1, and by presenting uncertainty budgets for the reference measurement chain for 53 Hz, 1 kHz, and 10 kHz frequencies for power factors 1.0 and 0.0.

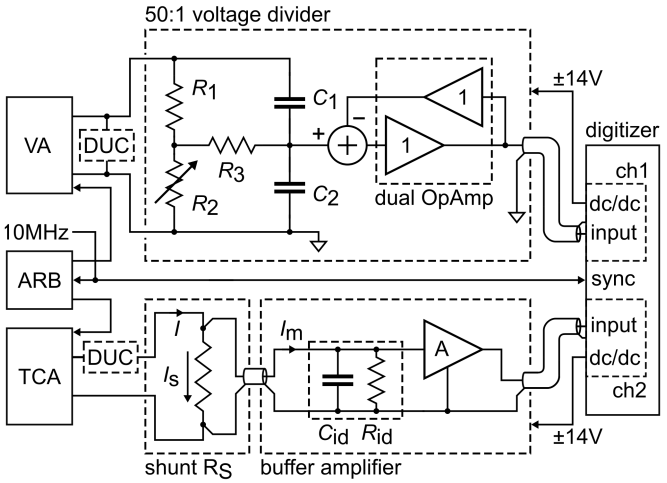

Fig. 1. Calibration setup for harmonic single-phase power. Signal generation (left), followed by the reference voltage and current transducers, and finally, the reference digitizer (right).

Bulding a custom digitizer design instead of using commercial off the shelf products guaranteed both the flexibility of the instrument and the right performance compromises in design. The custom digitizer has been previously reported [5], and it has proven to be versatile also outside power measurements. Recently, it has been updated to operate as a merging unit in accordance with IEC 61850-9-2LE and IEC 61869-9 standards [6]. It has six identical channels, two of which are used in this setup. Sampling is synchronized to the same 10-MHz reference signal driving the ARB. Power calculation runs on a PC, which calculates the harmonic power according to IEEE Std. 1459-2010 in the frequency domain [7].

III. Digitizer

A digital signal processor (DSP) card is used for collecting data from six analog input cards. The input signals are sampled with a maximum rate of 250 kHz. Circular buffers inside the DSP are emptied to a measurement PC via USB 2.0 such that constant gapless power analysis is possible on the PC. The software also estimates the input frequency from the data and constantly updates the 32-bit direct digital synthesis-based sample clock inside the digitizer. This operation forms a closed-loop system, which allows the measurement setup to

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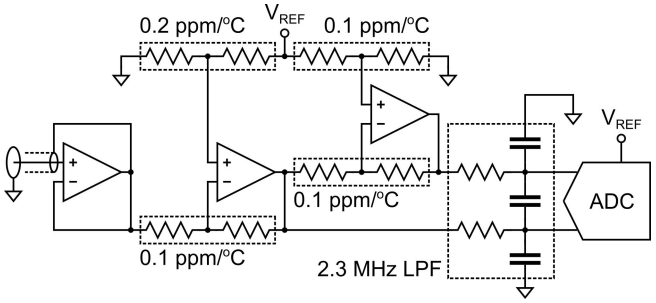

Fig. 2. Simplified schematic of ADC front end.

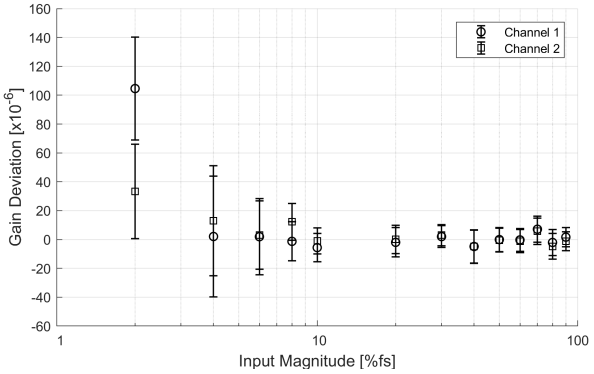

Fig. 3. Linearity of ADC channels one and two versus input magnitude in percents of full-scale (%fs) input at 1-kHz frequency. Error bars show type A uncertainty ($k = 2$).

track input frequency to sustain coherence between the input signal and the sampling frequency.

A. Design of Analog Input Channels

The most critical part of the digitizer affecting measurement uncertainty is the input channels. Choice of components in the front-end emphasizes low drift, good noise performance, and predictable frequency response. Built-in antialias filters were left out from the design, since pure signals generated in laboratory conditions guarantee aliasing-free sampling. The input channels are floating. Power is supplied with isolated ±15-V switch-mode supplies separately for each channel. The 15-V outputs are heavily filtered against common-mode noise, switching frequency fluctuation in the output voltage as well as switching transients caused by parasitic *LC* resonances inside the power supply module. The clean supplies are further filtered with high-bandwidth low dropout regulators to create the required operating voltages for analog and digital circuitries.

A simplified schematic of the analog input of a single channel is shown in Fig. 2. The input buffer is a low-noise, high-impedance FET-input operational amplifier (OpAmp) connected as a voltage follower. Input capacitance is reduced by driving the shield structure around the input connector and routing by the OpAmp output. The measured input capacitance of the input is 8.5 pF, consisting for the most part of the Bayonet Neill–Concelman connector and the OpAmp as well as the clamp diodes, which are not shown in the schematic.

The single-ended input is converted to a differential mode with a dual OpAmp circuit, which drives the analog-to-digital converter (ADC). The circuit has an attenuation of 4–1, which is set by 0.1 $\mu\Omega/\Omega/°C$ temperature coefficient (TC) tracking resistor networks. DC bias voltages at the OpAmp inputs are also set by resistor networks, which guarantee reasonably good dc performance. The ADC is an 18-bit successive approximation register-type device, with a 30-pF hold capacitor at its input. The driver OpAmps need to charge the capacitor between each sample, which may result in an excessive need for output current slewing. This is alleviated by placing a capacitor at the ADC input with a value roughly 10× higher than that of the hold capacitor [8]. Most of the charge flowing into the ADC input is then supplied by the capacitor. A small resistor is included for limiting the capacitive load for the OpAmps. This forms a low-pass filter with a cutoff frequency of roughly 2.3 MHz. Resistors and polyphenylene sulfide capacitors are handpicked in order to have a similar time constant in all six input channels.

Finally, in order to take full advantage of the low gain drift of the input circuitry, a low-drift 5.0-V full-scale voltage reference is designed. It comprises an ovenized Zener reference, a 0.2 $\mu\Omega/\Omega/°C$ TC tracking voltage divider, and low-drift buffers. Zener temperature is set to 50 °C, which, in practice, limits the operating temperature of the digitizer to 30 °C.

B. Measured Performance

Most importantly, the digitizer is characterized in terms of linearity, frequency response, channel-to-channel delay, and TC of gain. Noise performance is also important, but noise added to the input signal by the digitizer will simply manifest itself as additional type A uncertainty in the measurement result for a given measurement time. Good linearity even down to very small input magnitudes is desirable, since it means that, in practice, no level-dependent corrections for input gain are needed. Frequency response needs to be characterized in order to correct it at high frequencies. Large differences in delay between the channels would affect measured active power, especially at small power factors.

The linearity of input channels is tested using full-scale input voltage and 1-kHz frequency fed through an eight-decade inductive voltage divider (IVD). The division ratio of the IVD is adjusted from 90% down to 2%. Result for channels one and two is shown in Fig. 3. It can be seen that the gain remains within 7.1 10^{-6} above 10% and within 13 10^{-6} above 4% input magnitudes. Error bars in the figure represent only type A uncertainty of the measurement. A large part of the uncertainty is due to the short-term drift of the voltage source, which was not compensated. The IVD linearity is verified by comparing it against another eight-decade IVD of different makes. Division ratios of the two IVDs agree within $0.1 \cdot 10^{-6}$ for all tested ratios. The excellent linearity of the digitizer results in very small additional uncertainty on signal levels above 5% of full scale.

Frequency response is measured with an ac calibrator. The calibrator's output flatness is verified with MIKES ac voltage standard, which has an uncertainty of 8.0 μV/V for

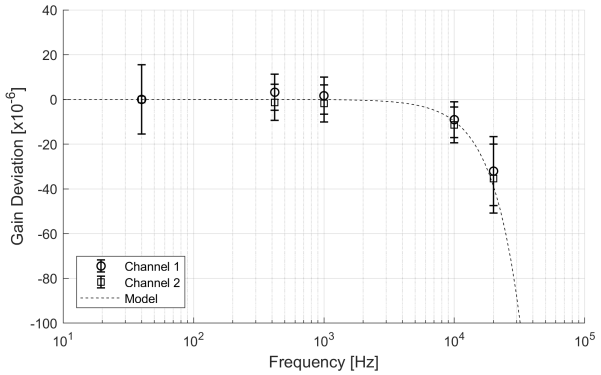

Fig. 4. Magnitude response of ADC channels one and two versus frequency. Dashed line: magnitude response of a first-order low-pass filter with a corner frequency of approximately 2.3 MHz. Error bars show overall uncertainty ($k = 2$) of the measurement.

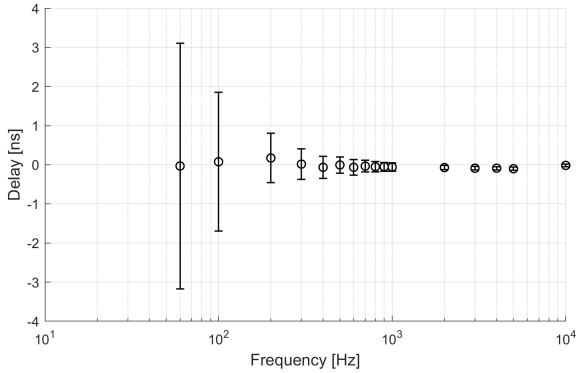

Fig. 5. Compensated phase delay between channels one and two using a 6.0-V input signal and 40960-Hz sampling rate. Error bars show only type A uncertainty of the measurement ($k = 2$).

absolute rms voltage magnitude for all frequencies used in the measurement. Fig. 4 shows the magnitude response of channels one and two. The plot includes a theoretical curve of a first-order low pass filter with a corner frequency of roughly 2.3 MHz at the ADC input. The filter was described in Section III-A. It can be seen that the measured response is very close to a simple model of the input circuit. It is, therefore, feasible to compensate the magnitude response in measurement software using the model. Corner frequency in the model can be adjusted to match the measurement result. The model can also be used to compensate for the phase response of the digitizer input, if an accurate representation of the input waveform is required. For determination of harmonic power, it is sufficient to measure the channel-to-channel phase response.

Since the digitizer was designed to have floating inputs, all digital lines between the ADC and the DSP were required to have data isolators. The isolators, which are used for connecting the sample clock to the ADCs, have a specification for unit-to-unit propagation delay skew of maximum 15 ns. This was clearly seen in the channel-to-channel delay measurement. All delays between the six channels were initially below 10 ns, which would contribute too much to the error budget at high frequencies and small power factors. It was found that the delays remain the same for all input frequencies. After determining the delays they were compensated in software and remeasured. Compensated phase delay between channels one and two is within 0.17 ns for all input frequencies, with -0.03-ns average and 0.07-ns standard deviation. The result can be seen in Fig. 5. The test was done with a 6.0-V input signal using 40960-Hz sample rate. All channels were connected to the same voltage source with equal-length coaxial cables.

The TC was measured in a temperature test chamber between 14.0 °C and 26.8 °C. The measured TC is (2.6 ± 0.2) and (2.2 ± 0.2) μV/V/°C for channels one and two, respectively.

IV. Current Shunts

Two different sets of custom shunts are used for current measurement. First set of six shunts with values of 75 mΩ, 100 mΩ, 200 mΩ, 500 mΩ, 1 Ω, and 2Ω for currents up to 20 A have been designed in house [9]. These shunts have a usable bandwidth up to 20 kHz. Long-term stability of this set appears to be extremely good. The 200-mΩ shunt has an average annual change of only -0.07 $\mu\Omega/\Omega$ from 2009 to 2017. The design incorporates forced airflow cooling, which results in excellent stability with respect to measurement current. The 200-mΩ shunt showed a temperature rise of 3.8 °C and relative resistance change of -0.2 $\mu\Omega/\Omega$/°C, when the test current was increased from 1.0 to 5.0 A. Small dependence from current and temperature means that it is not necessary to wait for the shunt to stabilize when changing the measurement current.

Another set of seven shunts were acquired from Justervesenet (JV), Norway, for a current up to 10 A. The design has previously been thoroughly tested and shows excellent performance with respect to ac–dc difference and phase response up to 100 kHz [10], [11].

A. Current Shunt Buffer Amplifiers

In order to avoid loading of the shunt, high input impedance buffers with different gains can be connected to its output. The buffers amplify the voltage sensed over the shunt. Unity gain stable OpAmps with 18-MHz gain bandwidth (GBW) product are used. Gains are set with 0.2 $\mu\Omega/\Omega$/°C resistance networks. The circuit uses a negative feedback scheme to improve phase accuracy at high frequencies [12]. The feedback system is drawn in detail in Fig. 1 in the voltage divider, which uses the same topology. High frequency rolloff and any temperature dependence of GBW is compensated by the feedback. This requires tight matching of the individual OpAmps, which can be guaranteed by using a dual OpAmp device. Buffers with gains of 1, 5, and 10 have been fabricated.

Fig. 6 shows the measured magnitude and phase responses of a buffer with a gain of 10. The measurement is done using an ac voltage standard. The gain measurement result is verified at 1-kHz frequency using an IVD to scale the output voltage of the buffer to the same level as the input, both of which are then measured with the ac voltage standard at the same input range. The results of the two measurements agree within the uncertainty of the first measurement.

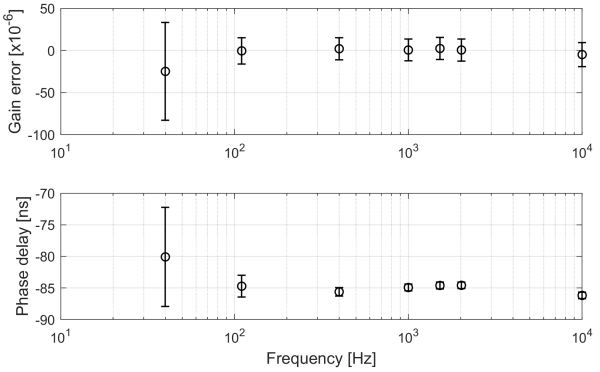

Fig. 6. Measured magnitude and phase responses of a buffer with a gain of 10. Error bars show overall uncertainty ($k = 2$) of the measurement.

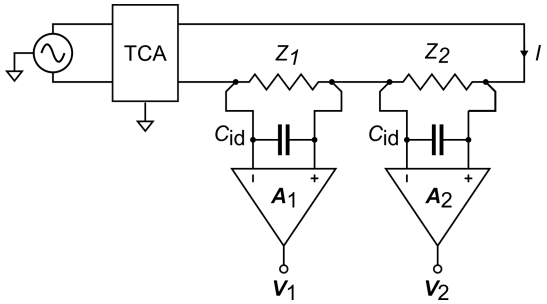

Fig. 7. Setup for step-up comparison of current shunts.

The latter result is used as a calibration coefficient for the buffer, since it has the smaller uncertainty of the two measurements. Phase response is determined with the digitizer using a 700-mV input signal by comparing buffer input and output phases. The phase delay remains relatively constant throughout the entire frequency range. The 10-kHz value for delay is used as a correction term, since an error in delay has the largest influence at high frequency. Similar characterization is done for other buffers. The buffer input capacitance C_{id} in Figs. 1 and 7 is 7.6 pF including adapters, which is small enough not to require correction through calculation even at 10 kHz.

B. Step-up measurement setup

Fig. 7 shows a setup for doing a step-up measurement of current shunts to transfer traceability from one shunt to another. Shunts Z_1 and Z_2 share the same test current I. Similar buffer amplifiers sense the voltages across the shunts. The digitizer is used for measuring the amplified voltages. Signal path gains include magnitude and phase angle errors, respectively, $\varepsilon_{\mathrm{A1}}$ and $\varepsilon_{\mathrm{A2}}$, and φ_{A1} and φ_{A2} resulting in complex gains

$$\boldsymbol{A}_1 = \varepsilon_{A1} A_1 e^{j(\varphi_{A1})} \text{ and } \boldsymbol{A}_2 = \varepsilon_{A2} A_2 e^{j(\varphi_{A2})}. \tag{1}$$

It should be noted that even though $\boldsymbol{A}_1$ and $\boldsymbol{A}_2$ are drawn as buffer gains only, in practice, they hold all possible errors for a given frequency for the entire measurement chain, i.e., from sensing the voltage across the shunt to digitizing the signals at the ADCs.

Errors in signal paths can be removed from the result by taking two sets of measurements of the voltage ratio. The first measurement is done according to Fig. 7 resulting in $\boldsymbol{V}_1 = \boldsymbol{Z}_1 \boldsymbol{A}_1 I$ and $V_2 = \boldsymbol{Z}_2 \boldsymbol{A}_2 I$, and the second one by exchanging the signal paths between the shunts such that $\boldsymbol{V'}_1 = \boldsymbol{Z}_1 \boldsymbol{A}_2 I$ and $\boldsymbol{V'}_2 = \boldsymbol{Z}_2 \boldsymbol{A}_1 I$. We may then expand the ratio of shunt impedances $\boldsymbol{Z}_1$ and $\boldsymbol{Z}_2$ and write it in Eulerian terms by

$$R_m e^{j\varphi} = \frac{\boldsymbol{Z}_2}{\boldsymbol{Z}_1} = \sqrt{\underbrace{\frac{\boldsymbol{Z}_2 \boldsymbol{A}_2 I}{\boldsymbol{Z}_1 \boldsymbol{A}_1 I}}_{meas1} \cdot \underbrace{\frac{\boldsymbol{Z}_2 \boldsymbol{A}_1 I}{\boldsymbol{Z}_1 \boldsymbol{A}_2 I}}_{meas2}} = \sqrt{\underbrace{\frac{\boldsymbol{V}_2}{\boldsymbol{V}_1}}_{meas1} \cdot \underbrace{\frac{\boldsymbol{V'}_2}{\boldsymbol{V'}_1}}_{meas2}} \tag{2}$$

where R_{m} and φ are, respectively, the ratio of magnitudes and the difference of phase angles of the two shunts. From (2), it follows that R_{m} is given by the geometric average of voltage magnitude ratios in the two measurements, that is,

$$R_m = \sqrt{\frac{V_2}{V_1} \cdot \frac{V_2^{'}}{V_1^{'}}} \tag{3}$$

and φ is given by the arithmetic average of the measured phase differences of voltage, that is,

$$\varphi = \frac{(\varphi_2 - \varphi_1) + (\varphi'_2 - \varphi'_1)}{2}. \tag{4}$$

V. Voltage Divider

A. Physical Design

The voltage divider is based on a capacitive divider with a resistive branch for low frequencies, followed by a compensated unity gain buffer, as shown in Fig. 1. Scale factor (S.F.) was chosen to be 50:1. The buffer uses the same topology as the buffers used with current shunt described in Section IV. At high frequencies, the divider is almost purely capacitive (C_1–C_2), while at 50 Hz, the resistive part (R_1–R_2–R_3) will slightly affect the division ratio. The aim is to maintain a steady rolloff from resistive to capacitive regions of operation. Therefore, a small part of R_2 is implemented as a trimmer for adjusting the ratio of the resistive part. R_3 is used for pushing the rolloff frequency down without having to use excessively large values for R_1 and R_2. In this design, the frequency of the transition between the two operation modes is 300 MHz.

The three-channel divider is housed inside a 19-in rack case. Only one of the channels is used in this setup. The dividers are in separate aluminum boxes inside the case, which isolates them from any external electric fields. Each divider can be powered externally by a laboratory supply. Alternatively, each channel can be powered separately using operating voltage fed by the digitizer thus establishing fully floating measurement chains. A small fan provides active cooling of the divider.

B. Measured Performance

S.F. error and phase delay of the voltage divider are shown in Fig. 8. They are measured using similar methods as for buffer amplifier as described in Section IV. Change in ratio and phase delay at low frequencies is due to mistuning of the resistive part. Change in ratio at high frequencies is due to the feedback scheme described in Section IV.

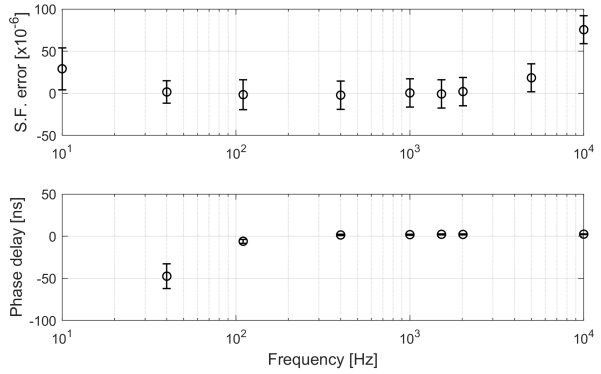

Fig. 8. Measured S.F. error and phase delay of a single voltage divider channel. Error bars show overall uncertainty ($k = 2$) of the measurement.

S.F. at 1 kHz is again verified with an IVD and both measurements are in perfect agreement. The IVD measurement result is used as a calibration coefficient. Since the input and output voltages of the divider are quite different, the phase response is further verified at 1 kHz with the same IVD. The IVD phase delay was first tested using the digitizer. The result showed better performance than what is the digitizer's channel-to-channel delay uncertainty, regardless of division ratio. The IVD was used for scaling the divider input voltage of 100 V such that two digitized channels had the same input magnitude. The result agrees with the 1-kHz result shown in Fig. 8.

For use in this setup, a single channel of the divider was also tested for temperature and voltage coefficients. In both test setups, the IVD was used as a reference by dividing the input voltage of the divider to the same level as the output voltage. Both voltages were then measured with the digitizer. The TC between 13.6 °C and 28.9 °C was measured in a temperature test chamber using 60-V input voltage. The test showed a TC of $(-0.3 \pm 0.2) \cdot 10^{-6}$/°C. Voltage coefficient was determined by measuring the division ratio at 1 kHz with test voltages 60, 100, and 200 V. The measurement showed slopes of $0.16 \cdot 10^{-6}$/V from 60 to 100V and $0.12 \cdot 10^{-6}$/V from 100 to 200 V. This should be taken into account as an uncertainty contribution unless different calibration coefficients for different input voltage levels are used.

VI. Uncertainty Budget

Uncertainty budgets in μW/VA are drawn up for frequencies 53, 1, and 10 kHz. Tables I and II, respectively, show the uncertainty contributions and combined uncertainties for power factors 1.0 and 0.0. Expanded uncertainties with coverage factor $k = 2$ are used in all cases. Magnitude errors are multiplied by a sensitivity coefficient $\cos(\varphi)$, where φ is the angle between voltage and current signals for a given power factor [1]. For phase angle errors the sensitivity is $\sin(\varphi)$.

The laboratories in MIKES are temperature stabilized, which means that a temperature variation of 0.5 °C can be considered very conservative. In practice, the laboratory air is constantly within 0.2 °C but a higher number allows for local differences due to nearby heat sources.

TABLE I
Uncertainty Budget for Power Factor = 1.0.
Uncertainties Are Given as Parts in 10^6.

Uncertainty component	53 Hz	1 kHz	10kHz
Digitizer, two channels combined			
Calibration (53 Hz)	11.5	11.5	11.5
Linearity (10% …100%)	18.1	18.1	18.1
Compensated magnitude response	0.0	11.3	11.3
Channel synchronicity	0.0	0.0	0.0
Temperature coefficient (±0.5°C)	3.4	3.4	3.4
Voltage divider			
Calibration (100V, 1 kHz)	0.5	0.5	0.5
Voltage dependence	6.5	6.5	6.5
Compensated magnitude response	13.4	0.0	16.7
Compensated phase displacement	0.0	0.0	0.0
Temperature coefficient (±0.5°C)	0.3	0.3	0.3
Current shunt			
Calibration (DC)	1.6	1.6	1.6
AC-DC difference [a]	5.0	10.0	10.0
phase displacement	0.0	0.0	0.0
Temperature coefficient (±0.5°C)	0.2	0.2	0.2
Current shunt buffer (1x/5x/10x)			
Calibration (53 HZ & 1 kHz)	2.9	2.9	2.9
magnitude response	3.3	0.0	1.0
phase response	0.0	0.0	0.0
TOTAL $k = 2$ (μW/VA)	27.2	27.4	32.1

[a] Preliminary numbers.

TABLE II
Uncertainty Budget for Power Factor = 0.0.
Uncertainties Are Given as Parts in 10^6.

Uncertainty component	53 Hz	1 kHz	10kHz
Digitizer, two channels combined			
Calibration (53 Hz)	0.0	0.0	0.0
Linearity (10% …100%)	0.0	0.0	0.0
Compensated magnitude response	0.0	0.0	0.0
Channel synchronicity	0.1	1.3	12.6
Temperature coefficient (±0.5°C)	0.0	0.0	0.0
Voltage divider			
Calibration (100V, 1 kHz)	0.0	0.0	0.0
Voltage dependence	0.0	0.0	0.0
Compensated magnitude response	0.0	0.0	0.0
Compensated phase displacement	9.8	7.5	62.8
Temperature coefficient (±0.5°C)	0.0	0.0	0.0
Current shunt			
Calibration (DC)	0.0	0.0	0.0
AC-DC difference	0.0	0.0	0.0
phase displacement [a]	53.9	53.9	124.5
Temperature coefficient (±0.5°C)	0.0	0.0	0.0
Current shunt buffer (1x/5x/10x)			
Calibration (53 HZ & 1 kHz)	0.0	0.0	0.0
magnitude response	0.0	0.0	0.0
phase response	2.7	6.3	62.8
TOTAL $k = 2$ (μW/VA)	54.8	54.8	153.5

[a] Preliminary numbers.

Since the setup uses two channels, all tabulated uncertainty components for the digitizer except for channel synchronicity represent the combined uncertainty of the two channels. Channel synchronicity represents the difference in phase angle between the two channels, and is thus included only once. Calibration of the digitizer is traceable to an 8½-digit sampling voltmeter at 53 Hz and for higher frequencies,

the frequency response measurement is used with uncertainties shown in Fig. 4. For the voltage divider, calibration is performed at 100 V and 1 kHz and it is traceable to an IVD. For other voltages and frequencies, the voltage coefficient and uncertainty in magnitude response need to be taken into account. Current shunts still lack traceability for their ac–dc difference, and the tables show preliminary numbers based on the JV shunts published in [10] and [11]. The associated buffer amplifiers contribute to uncertainty mostly at small power factors. Numbers in Tables I and II are for a unity gain buffer.

VII. Conclusion

A single-phase calibration setup for calibration of voltage, current, power, power factor, and power harmonics is presented. A phantom power source is used for the generation of the test signals. The setup can be used for calibration on voltages up 350 V and currents up to 20 A, and uncertainties are estimated for frequencies from 53 Hz to 10 kHz. Measurement is based on capacitive–resistive voltage dividers, two different designs of resistive current shunts, and a custom digitizer. Magnitude and phase errors of reference voltage and current sensors and digitizer inputs are determined and compensated in measurement software. Other uncertainty contributions, such as temperature, voltage, and current coefficients are small enough so that they do not need corrections. Instead, they are added into the uncertainty budget.

The system can measure power with an expanded uncertainty of 32 μW/VA on unity power factor up to 10 kHz. With smaller power factors the uncertainty increases so that at 10 kHz the uncertainty is 158 μW/VA on zero power factor. Work is still needed for establishing traceability to the current measurement.

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