

**VTT**

# **Silicon photonics MPW offering 2021**

# VTT's open access multi-project wafer runs for 3 $\mu\text{m}$ silicon photonics platform

Runs are optimal for low-cost, low-barrier prototyping and evaluation of photonic integrated circuits.

## Design support

A process design kit (PDK) is offered to multi-project wafer run (MPW) participants to assist in the design work. The documentation describes the layout design guidelines and the design rules. VTT also offers layout design as an additional service.

## Pricing model

Pricing is based on the choice of the design area size and the

process module combination and includes the delivery of several identical chips. Additional chips can be provided for additional cost.

## Process modules

The process can be chosen from three alternative modules: passive, active, and Ge-PD. Planarization (for routing electrical wires on the chip) and solder plating (for flip-chip integration of active components) are also available for extra cost.

## Deadlines

The MPW registration deadline is one month before the design deadline. In case the mask design is not delivered before the design deadline to VTT, there will be a one-time option to postpone participation to the next suitable run for a small transfer fee.

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## How to join

You can express your interest in joining an MPW run by sending an email to [silicon.photonics@vtt.fi](mailto:silicon.photonics@vtt.fi). Access to the PDK documentation requires signing a design kit license agreement (DKLA) with VTT.



Design Area	Base Price (BP) of Module			Delivered Chips	Chips for Additional 50% BP
	Passive	Active	Ge-PD		
5 × 4.75 mm <sup>2</sup>	7 k€	11 k€	20 k€	5	+5
5 × 9.5 mm <sup>2</sup>	11 k€	16 k€	35 k€	10	+10
20 × 19.5 mm <sup>2</sup>	30 k€	45 k€	71 k€	3	+3


Design Deadline	Included Modules		
	Passive	Active	Ge-PD
5 January	✓	✓	✓
16 May	✓	✓	
3 October	✓	✓	✓

**Passive module** includes the basic rib and strip silicon waveguide processing. Also provided are Al-coated facet reflectors for resonators and echelle gratings. For coupling both etched waveguide facets and up-reflecting mirrors are available with AR-coating for 1310 nm or 1550 nm.

**Active module** has the same process steps as the passive module, but adds Al for electrical wiring and silicon implantation (p- and n-type) steps for thermo-optic and PIN phase shifters.

**Ge photodiodes module** extends the offering of the active module by providing also the photodiode process. Separate designs are available for <1 GHz monitor and for fast photodiodes.



**For technical reference see  
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JSTQE.2019.2908551** 

AALTO ET AL.: "OPEN-ACCESS 3-UM SOI WAVEGUIDE PLATFORM FOR DENSE PHOTONIC INTEGRATED CIRCUITS"

The logo for VTT, consisting of the letters 'VTT' in a bold, white, sans-serif font, centered within an orange square.

**VTT**

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